

Attorney's Docket No.: 10559-317001/P9678

REMARKS

Claims 1-7, 15-26, and 30-34 are pending. Claims 32-34 have been added. Claims 1, 15, and 19 are in independent form.

Applicant thanks the Examiner for the courtesy of the telephone discussions conducted on April 12, 2006 and April 13, 2006, at which time arguments as hereinafter developed were presented. Further, how a plurality of two-ported random access memory devices can be used to build a general purpose register set that comprises two effective read ports and one effective write port was also discussed, with reference to FIGS. 3 and 6 and the written descriptions thereof.

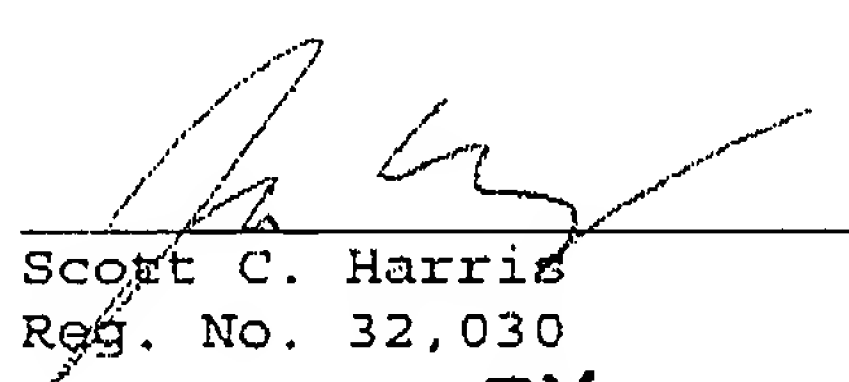
The present claims have been amended to further clarify what is meant by an "effective write port." For example, claim 1 has been amended to recite that the arithmetic logic unit can write to each bank in the general purpose register set using the one effective write port. As another example, claim 19 has been amended to recite a data link between the arithmetic logic unit and the one effective write port of the general purpose register set. The data link allows the arithmetic logic unit to write to different two-ported random access memory devices through the one effective write port.

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As discussed in the response filed February 17, 2006, none of the cited references describe or suggest a register set that comprises a plurality of two-ported random access memory devices and includes two effective read ports and one effective write port. Indeed, one of the cited references (i.e., Parady) acknowledges that multi-ported register files can occupy more silicon than simple duplication of registers and thus clearly considers them to be distinct.

Accordingly, Applicant submits that claims 1, 15, and 19 and the claims dependent therefrom are patentable over the cited references. Applicant thus asks that all claims be allowed. No fees are believed due at this time. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: July 21, 2006

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